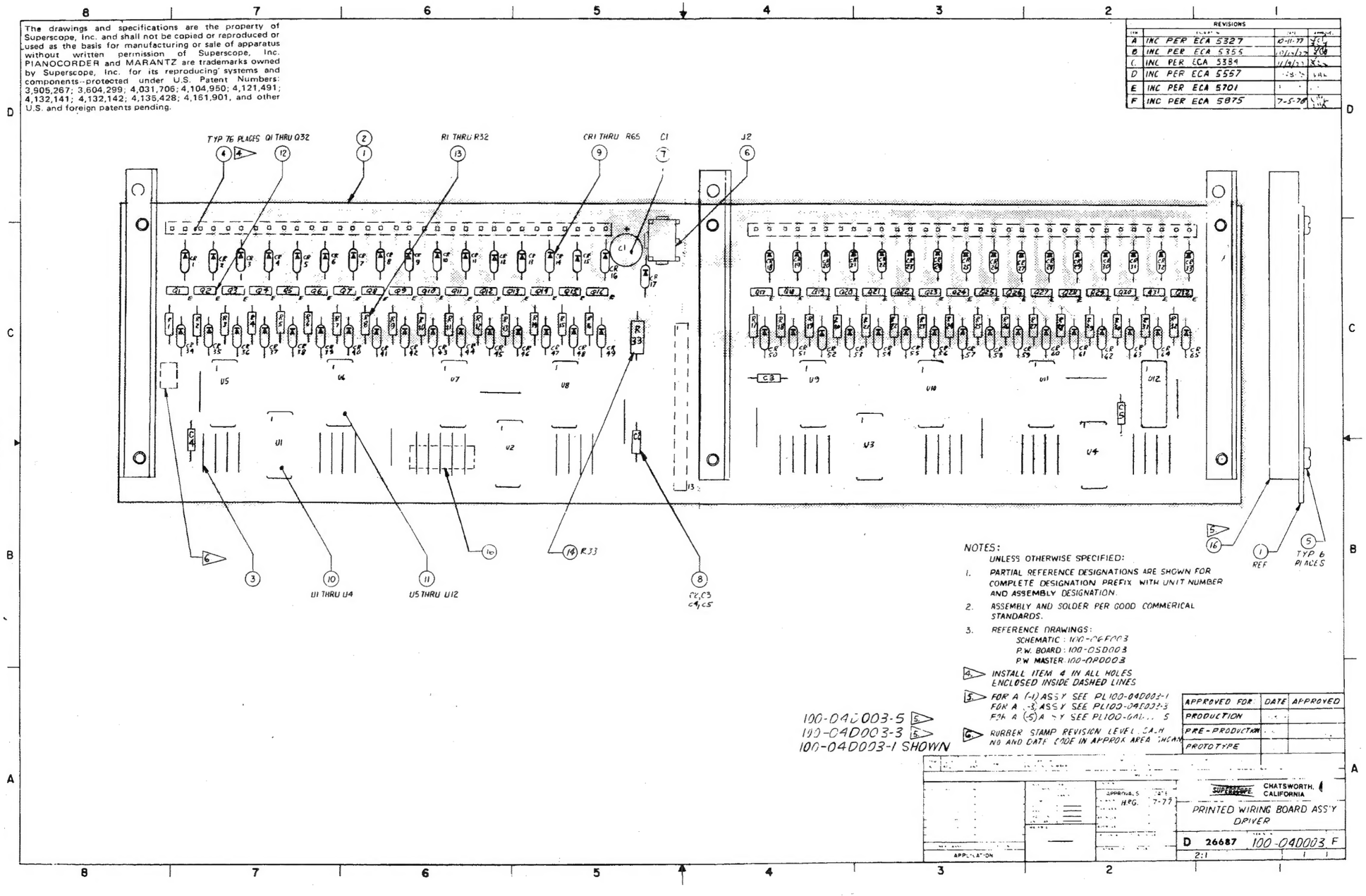
FIGURE 16-A






| REVISIONS | | | |
|---|---|---|---|
| LTR | | | |
| A | INC PER ECA 5327 | 10-11-77 | |
| B | INC PER ECA 5355 | 12/12/77 | |
| C | INC PER ECA 5389 | 1/9/78 | |
| D | INC PER ECA 5557 | | |
| E | INC PER ECA 5701 | | |
| F | INC PER ECA 5875 | 7-5-78 | |

NOTES:
UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ASSEMBLY AND SOLDER PER GOOD COMMERICAL STANDARDS.
3. REFERENCE DRAWINGS:
   SCHEMATIC : 100-06F003
   P.W. BOARD : 100-05D003
   P.W MASTER 100-04D003
4. INSTALL ITEM 4 IN ALL HOLES ENCLOSED INSIDE DASHED LINES
5. FOR A (-1) ASSY SEE PL100-04D003-1
   FOR A (-3) ASSY SEE PL100-04D003-3
   FOR A (-5) ASSY SEE PL100-04D003-5
6. RUBBER STAMP REVISION LEVEL, DASH NO AND DATE CODE IN APPROX AREA SHOWN

100-04D003-5
100-04D003-3
100-04D003-1 SHOWN

| APPROVED FOR | DATE | APPROVED |
|---|---|---|
| PRODUCTION | | |
| PRE-PRODUCTION | | |
| PROTOTYPE | | |

APPLICATION

APPROVALS REQ. 2:1 7-79

SUPERSCOPE CHATSWORTH, CALIFORNIA

PRINTED WIRING BOARD ASS'Y DRIVER

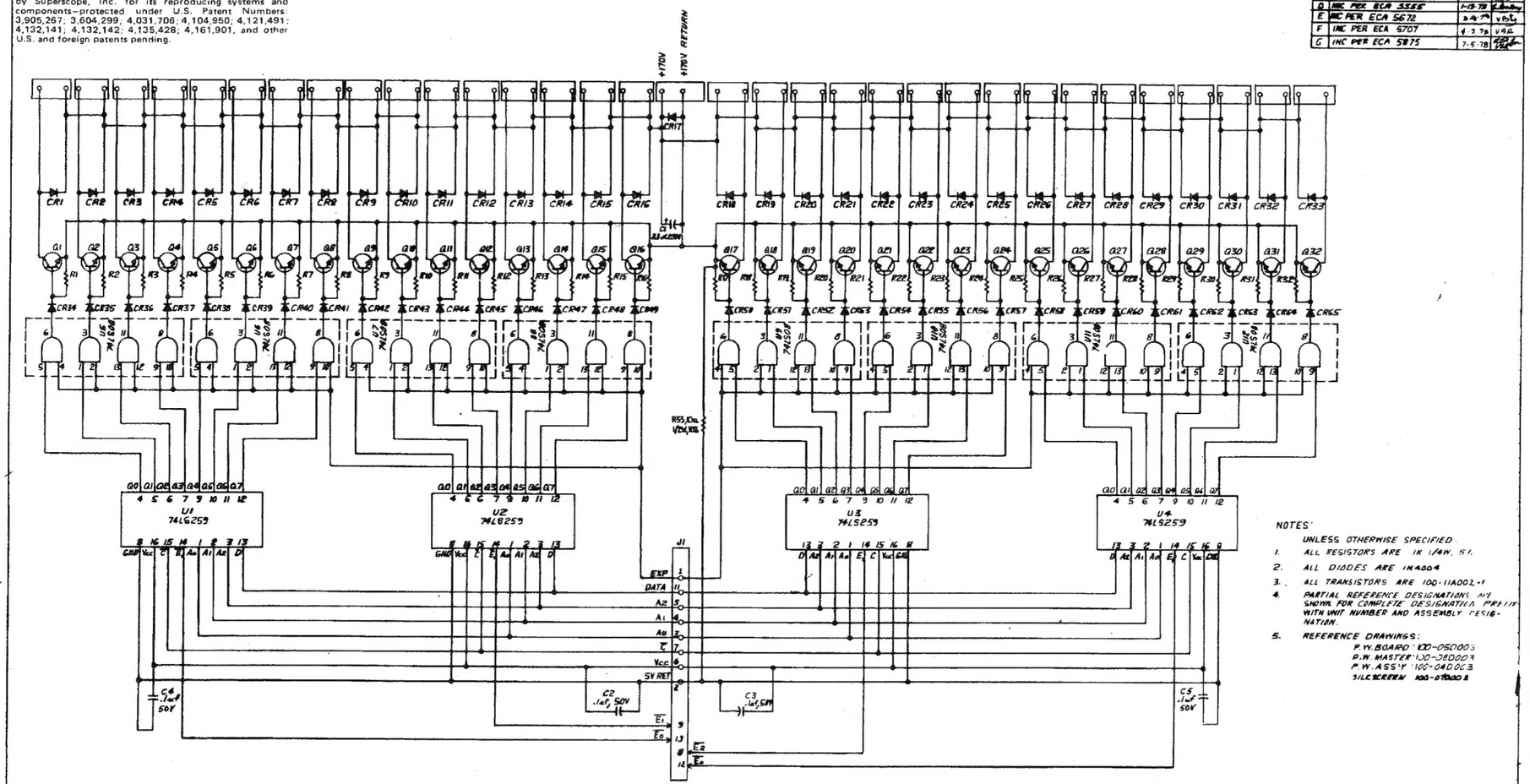
D 26687 100-04D003 F

2:1

FIGURE 16-B



| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPROVED |
| A | INC PER ECA 3935 | 10/14/77 | |
| B | INC PER ECA 5384 | 11/14/77 | |
| C | INC PER ECA 5511 | 12-28-77 | |
| D | INC PER ECA 3565 | 1-13-78 | |
| E | INC PER ECA 5672 | 3-9-78 | |
| F | INC PER ECA 6707 | 4-3-78 | |
| G | INC PER ECA 5875 | 7-5-78 | |




NOTES:

UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1K 1/4W, 5%.
2. ALL DIODES ARE 1N4004
3. ALL TRANSISTORS ARE 100-11A002-01
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.
5. REFERENCE DRAWINGS:
   P.W. BOARD: 100-05D003
   P.W. MASTER: 100-08D009
   P.W. ASS'Y: 100-04D003
   SILKSCREEN: 100-07D003

| | GND | VCC |
|---|---|---|
| U5 | 7 | 14 |
| U6 | 7 | 14 |
| U7 | 7 | 14 |
| U8 | 7 | 14 |
| U9 | 7 | 14 |
| U10 | 7 | 14 |
| U11 | 7 | 14 |
| U12 | 7 | 14 |

| APPROVED FOR | DATE | APPROVED |
|---|---|---|
| PRODUCTION | 1-26-78 | |
| PRE-PRODUCTION | 9-21-77 | |
| PROTOTYPE | | |

| QTY PER BOARD | SYM | CODE IDENT | PART OR IDENTIFYING NUMBER | NOMENCLATURE OR DESCRIPTION | MATERIAL OR REFERENCE DESIGNATION | SPECIFICATION | ITEM NO. |
|---|---|---|---|---|---|---|---|

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
REMOVE ALL BURRS
BREAK SHARP EDGES
MEET DIM. BEFORE/AFTER FINISH

| HOLE DIA. | TOLERANCE |
|---|---|
| .0938 THRU .128 | +.004 - .001 |
| .136 THRU .368 | +.005 - .001 |
| .221 THRU .359 | +.006 - .001 |
| .397 THRU .703 | +.008 - .001 |
| .75 THRU 1.000 | +.014 - .001 |
| 1.031 THRU 2.000 | +.012 - .001 |

DECIMAL .XX ± .XXX ANGULAR ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

LIST OF MATERIAL
CONTRACT NO.

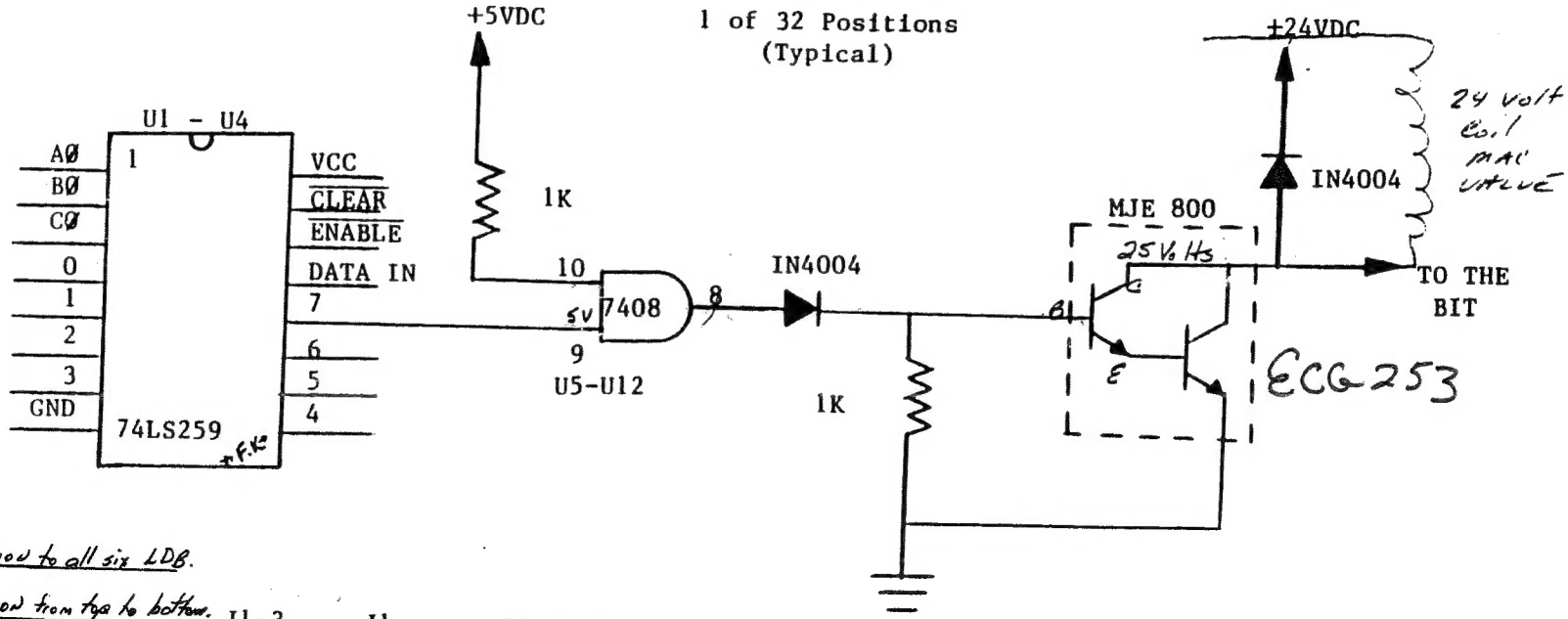
| APPROVALS | DATE |
|---|---|
| DESIGN SYM NUEMELI | 7-18-77 |
| CHECK | |
| APPROVAL | |
| APPROVAL | |
| DESIGN ACTIVITY APPROVAL | |
| CONTRACTOR APPROVAL | |

SUPERSCOPE CHATSWORTH, CALIFORNIA

SCHEMATIC
DRIVER

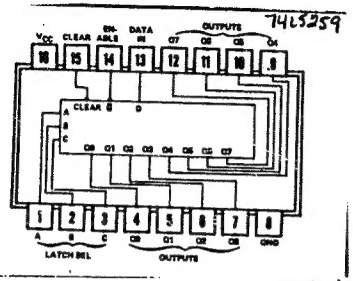
SIZE F | CODE IDENT NO. 26687 | DRAWING NO. 100-06F003 | REV. G
SCALE NONE | SHEET 1 OF 1

# LONG DRIVER BOARD SCHEMATIC (Partial)




- Address lines are common to all six LDB.
- ENABLE lines are common from top to bottom.

| J1-3 | J1 | ON BOARD TIE POINTS |
|---|---|---|
| | 1 | GND |
| | 2 | PIN 1 U1 - U4 |
| 47 | 3 | PIN 2 U1 - U4 |
| 46 | 4 | PIN 3 U1 - U4 |
| 45 | 5 | VCC (+5VDC) |
| 48 | 6 | PIN 15 U1 - U4 |
| 22 | 7 | PIN 14 U3 |
| 19 | 8 | PIN 14 U2 |
| 18 | 9 | KEY |
| | 10 | PIN 13 U1 - U4 |
| 21 | 11 | PIN 14 U4 |
| 20 | 12 | PIN 14 U1 |
| 17 | 13 | |




4 ENABLE LINES PER LDB.

12 ENABLE LINES PER DRAWER

3 Address LINES

2 DATA LINES

## 74LS259 TRUTH TABLES

**FUNCTION TABLE**

| INPUTS CLEAR | INPUTS $\overline{G}$ | OUTPUT OF ADDRESSED LATCH | EACH OTHER OUTPUT | FUNCTION |
|---|---|---|---|---|
| H | L | D | $Q_{i0}$ | Addressable Latch |
| H | H | $Q_{i0}$ | $Q_{i0}$ | Memory |
| * L | L | D | L | 8-Line Demultiplexer |
| L | H | L | L | Clear |

**LATCH SELECTION TABLE**

| SELECT INPUTS C | B | A | LATCH ADDRESSED |
|---|---|---|---|
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

H = high level, L = low level
D = the level at the data input
$Q_{i0}$ = the level of $Q_i$ (i = 0, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.